Optimum ArFi light source bandwidth for 10nm node logic imaging performance

Paolo Alagna[a], Omar Zurita[b], Vadim Timoshkov[c], Patrick Wong[d]
Greg Rechtsteiner[b], Jan Baselmans[c], Julien Mailfert[d]

a) Cymer LLC, Kapeldreef 75, 3001 Leuven, Belgium

b) Cymer LLC, 17075 Thornmint Court, San Diego, CA 92127

c) ASML Netherlands B. V. De Run 6501, 5504 DR Veldhoven, The Netherlands

d) imec, Kapeldreef 75, 3001 Leuven, Belgium

ABSTRACT

Lithography process window (PW) and CD uniformity (CDU) requirements are being challenged with scaling across all device types. Aggressive PW and yield specifications put tight requirements on scanner performance, especially on focus budgets resulting in complicated systems for focus control. In this study, an imec N10 Logic-type test vehicle was used to investigate the E95 bandwidth impact on six different Metal 1 Logic features. The imaging metrics that track the impact of light source E95 bandwidth on performance of hot spots are: process window (PW), line width roughness (LWR), and local critical dimension uniformity (LCDU).

In the first section of this study, the impact of increasing E95 bandwidth was investigated to observe the lithographic process control response of the specified logic features. In the second section, a preliminary assessment of the impact of lower E95 bandwidth was performed. The impact of lower E95 bandwidth on local intensity variability was monitored through the CDU of line end features and the LWR power spectral density (PSD) of line/space patterns. The investigation found that the imec N10 test vehicle (with OPC optimized for standard E95 bandwidth of300fm) features exposed at 200fm showed pattern specific responses, suggesting areas of potential interest for further investigation.

1. INTRODUCTION

To meet demanding market requirements and to enable low k1 printability, ArF immersion lithography must overcome significant challenges in patterning. Among all of the resolution enhancement techniques, multiple patterning is the most widely used and is considered to be the fundamental enabler for extending printability and device scaling. As forecast by the ITRS technology roadmap (see Table 1), process control plays a crucial role in high volume manufacturability of future DUV lithographic nodes.

	Table LITH2 Lithography Difficult Challenges
	Near Term Challenges (2013–2016)
1	Cost and cycle time of multiple patterning – especially for more than 2x
2	Process control on key parameters such as overlay, CD control, LWR with multiple patterning
3	EUV Source power
4	EUV Mask Infrastructure (defect inspection and verification, mitigation, mask lifetime) Defect free EUV mask blanks, mask availability
5	EUV resist and/or process that meets sensitivity, resolution, LER requirements
6	DSA defectivity and positional accuracy

Table 1. 2013 ITRS Technology Roadmap: 2013-2016 top lithographic challenges [1]

This study will focus on the E95 bandwidth sensitivity of a Metal 1 layer for a N10 (10nm) Logic node as engineered at imec as part of a LELELE triple patterning process. Estimates of on product focus budgets

are in the range of 40nm to 60 nm, (Table 2) requiring a comprehensive study of all known focus contributors and adjustment capabilities (i.e. knobs) in order to deliver optimal patterning results. Previous studies [2-5] have demonstrated the importance of monitoring light source performances to maintain optimal process stability.

HVM Roadmap	2014	2015	2016	2017	2018
Logic Foundry	20nm	16 / 14nm	10nm		7nm
Logic MPU	22nm 14nm		10nm		7nm
DRAM	D2xL	D2xL	D1xH		D1xM
Flash	16nm & 3D 24	16nm & 3D Gen 2	1xL | 3D-Gen 3	1yL | 3D Gen 4	
On Product Overlay [1]	5.0 ~ 4.0nm	4.5 ~ 4.0nm	4.0 ~ 3.5nm	3.5 ~ 3.0nm	3.0 ~ 2.5nm
On Product Focus [2]	90nm ~ 60nm	80nm ~ 60nm	70nm ~ 60nm	~ 60nm	~ 50nm

[1] Range for Memory & Logic critical layers [2] Range for EUV & ArF immersion foundry production wafer focus control requirements with process window enhancement techniques.

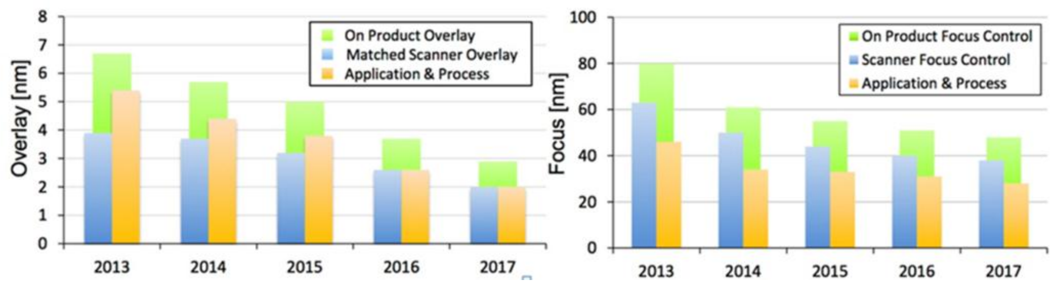

Table 2. Technology Overlay and Focus budged prediction[6]

For multiple patterning based Logic devices, the optimal printability is not only driven by the optimization of the optical proximity correction (OPC), but also by complex process factors, such as resist, exposure tool, and mask-related error performance levels. In addition the light source plays a crucial role; it has been widely demonstrated[7-11] how changes in the E95 bandwidth can significantly lead to changes in on wafer patterning due image contrast changes.

Logic patterns designed for triple patterning applications (like the one considered in this study) utilize complex OPC structures, increasing the difficulty in predicting changes in Critical Dimension (CD) due to E95 bandwidth when compared to basic line and space [4] structures, as summarized in in Figure 1.

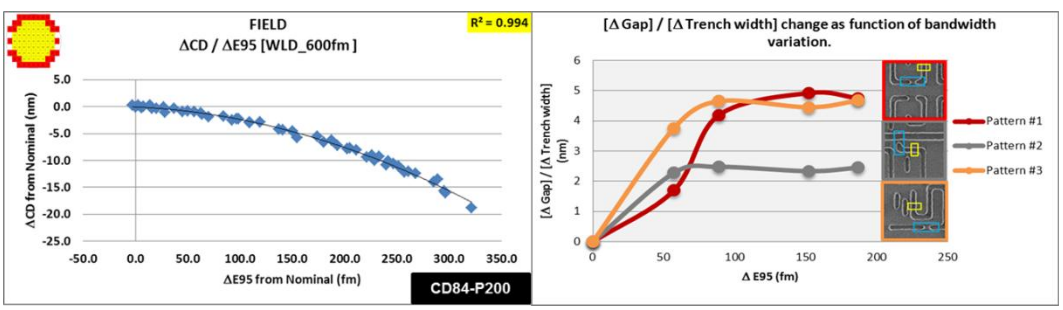

Figure 1. Different CD response of standard line-space and logic patterns with complex OPC

To facilitate study of the impacts of light source performance on patterning, Cymer has developed an engineering approach to enable modulation of light source optical parameter performance to a high degree of accuracy and precision at the wafer, exposure field, and intra-field levels (see Figure 2). This methodology has been reported in previous studies[4] and was successfully used to identify 1D and 2D pattern sensitivities to changes in E95 Bandwidth, Wavelength Sigma, and Energy Sigma. In collaboration with Chipmakers, Cymer has applied this methodology to characterize the critical layer performance of multiple devices (logic, memory, and foundry) as a function of changes in optical parameters. Use of this capability enables Cymer and Chipmakers to easily study and identify light source critical performance deviations which can have an impact on yield.

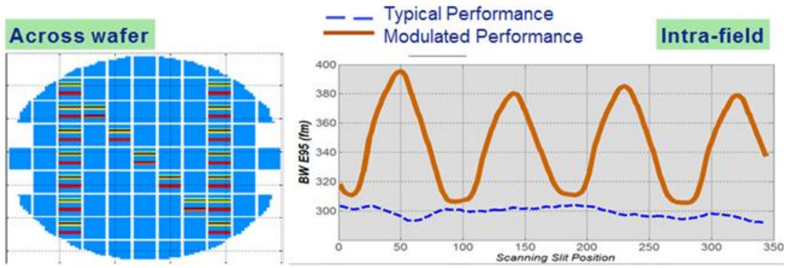

Figure 2. An example of Cymer's optical parameter modulation capability

2. EXPERIMENT CONDITION AND RESULTS

A set of experiments was conducted at imec's facilities in Leuven (Belgium) using an ASML immersion scanner model NXT:1950i connected to a Cymer XLR-660ix light source. A triple patterning (LELELE) N10 Metal 1 layer with tightest pitch of 48 nm was selected as a representative candidate for 10nm Logic node patterning in this experiment. The test vehicle mask offers a wide selection of patterns for study, as shown in Figure 3.

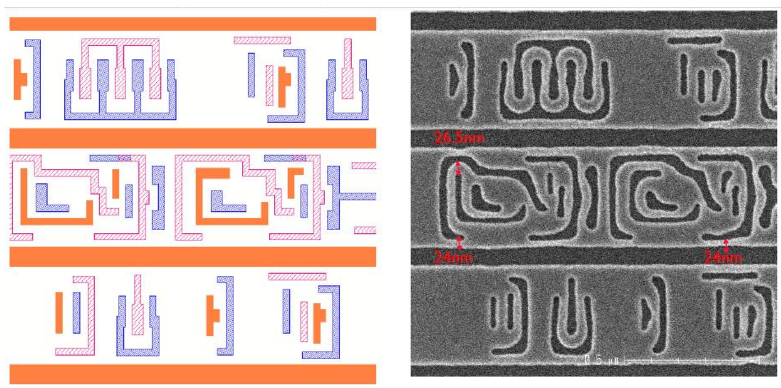

Figure 3. Subset of the available features on the imec N10 test vehicle

Among all the available logic features on the IMEC test mask, the 6 critical structures or Hot Spots (HS) showing the most intense focus sensitivity were selected. (Figure 4).

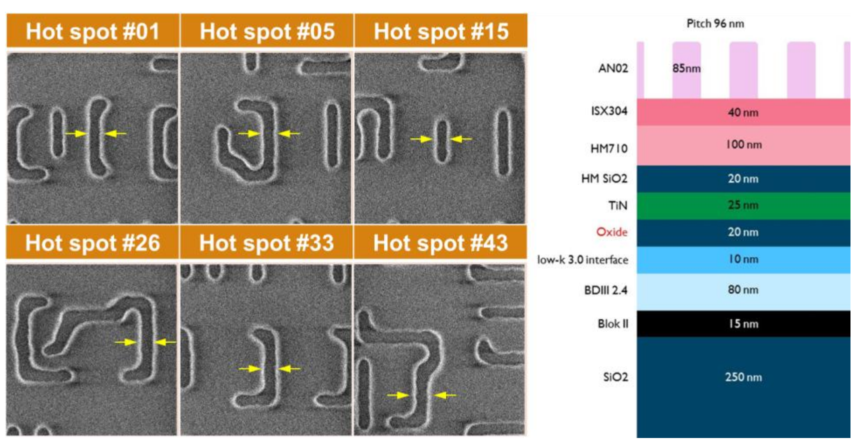

Figure 4. Features measured and process stack used in this study

It should be noted that this study has focused on a single test vehicle mask that is part of a larger LE^3 flow. The work presented in this paper can be considered then as the subset of a broader project which would include the study of E95 bandwidth changes through the entire LELELE (LE^3) flow. For this reason

experimental samples were prepared using the substrates optimized for the triple patterning process (see Figure 4); note that a TiN hard mask (HM) would be used for the final LE^3 pattern transfer.

Additional details on the CD targets are provided below:

- Anchor Feature: Line Space CD 45 nm Pitch 96 nm on mask;
- After Development Inspection (ADI) CD Target: 39nm trench in NTD resist;
- CD Target at TiN: 24nm;
- Litho-Etch shrink by tapered SOG etch: 15nm;
- After Etch Inspection (AEI) CD Target Range: ± 3nm.

This study included analysis of E95 bandwidth ADI responses in the following areas:

- Defect Density;
- Hot spot Process Window and Exposure Latitude (EL);
- Tip-to-Tip CD and LCDU Response;
- CD Contour analysis;
- Line-Space LWR (in the spatial domain).

2.1 Light Source E95 Bandwidth Modulation

In this study, the light source E95 bandwidth performance was modulated on a per wafer basis. Figure 5 shows the E95 bandwidth measured at wafer level. Note: despite the non-standard E95 bandwidth performance settings, no degradation in light source stability was detected; for example, 187 exposure fields were measured across each wafer and the 3 sigma of E95 bandwidth was in the range of 10fm to 25fm.

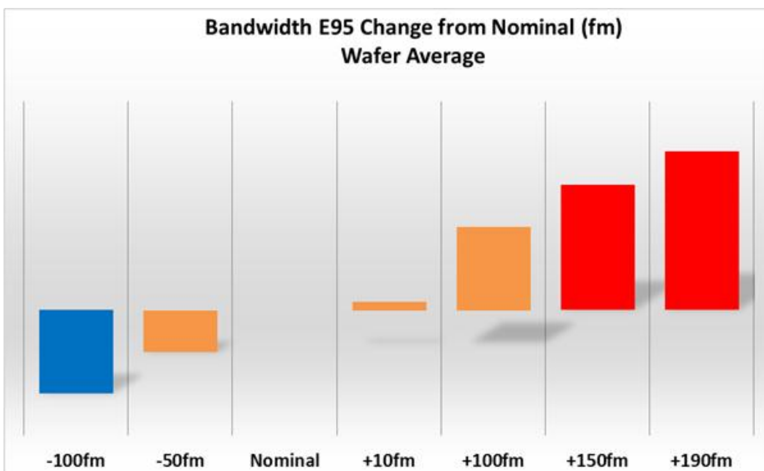

Figure 5. Bandwidth E95 set value (wafer average)

The different E95 bandwidth set points were selected to ensure a comprehensive study across a wide range of performance. To the authors' knowledge, this data in this study is the first investigation of the impact of lower E95 bandwidth (E95 < 300 fm) on advanced process node patterning.

2.2 Defect Density

To gain an understanding of the overall impact of E95 bandwidth changes on certain critical features, defect inspection was done using a broadband plasma inspection system from KLA Tencor. By using the bright field mode of the tool, a maximum capture rate of the defective critical features was achieved. The total area of the inspection was around 0.85 cm^2. Figure 6 shows that patterning impacts are detected at elevated E95 bandwidth values (in the range of 100fm to 150fm).

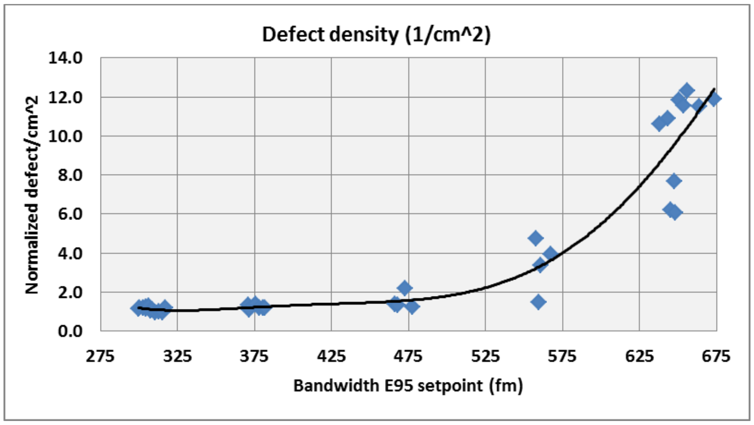

Figure 6. KLA 2835 defect density inspection results

2.3 Anchor feature

As reported in a previous study[4] , dense line-space features have limited sensitivity to contrast changes; this was confirmed in this experiment through the measurements performed on the anchor feature (CD 40nm Pitch 96 nm). It was determined that the target feature would experience meaningful changes in the process window only when the bandwidth deviation from nominal value exceed +100fm. In addition, looking at Figure 7, it is clear that changes in the E95 bandwidth reduce the usable process window due to an induced shift. Analysis with the reference exposure dose and focus constant shows a reduction in CD, whereas analysis with a fixed CD target shows a shift in the exposure dose. In both cases the rate of change is largest between nominal and 100fm. If the shift occurs due to long term E95 drift, perhaps on-line feedback control could be used to compensate; however, if the bandwidth change is more rapid, as would be the case in a within wafer excursion, this change would not be correctable using an advanced process control method.

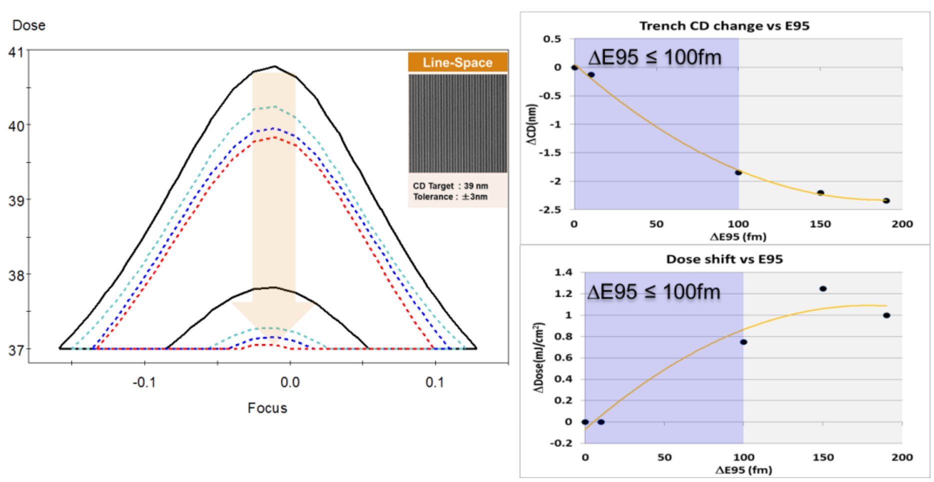

Figure 7. Anchor feature CD 40 nm Pitch 96 nm

2.4 Hot spot Process Window and Exposure Latitude (EL)

The effect of E95 bandwidth changes, an analog for potential drifts or excursions that could occur during production, on hot spots was studied using a "common process window" analysis. The "common process window" refers to the ranges of doses and focus over which a selected number of features can be patterned within CD specification. For the process window analysis at all E95 bandwidth conditions, wafers were exposed using a Focus Exposure Matrix (FEM) layout with steps of 0.5mJ/cm^2 in dose and 20nm in focus. Four CD measurements per exposure field were made using a Hitachi CG5000 CD-SEM.

The results summarized in Figure 7 show that E95 bandwidth should be controlled within 10fm to ensure negligible process variability. It can also be noted that a significant reduction in exposure latitude results from an increase in E95 bandwidth.

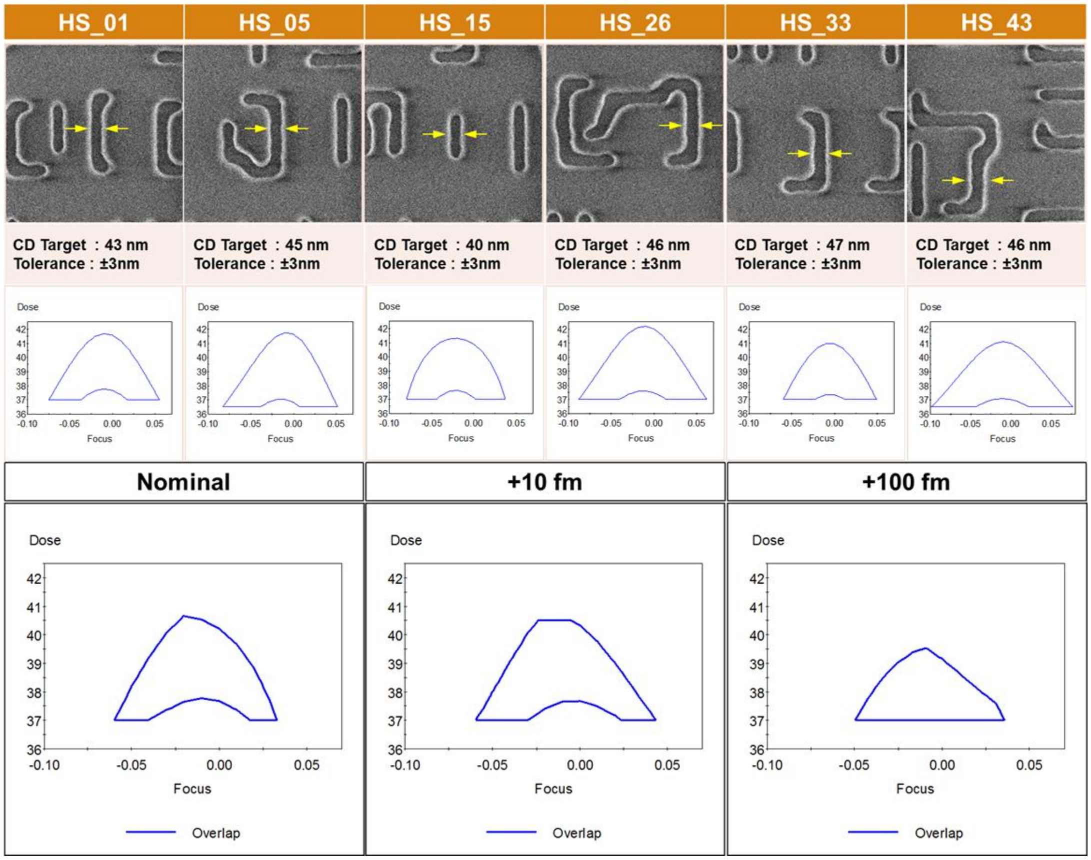

Figure 7. Hot spots common process window

Close inspection of the results reveals that the E95 bandwidth response varies from hot spot to hot spot (as shown in Figure 8). This confirms that, unlike the predictability of the line-space structures, the patterning response of 2D logic features is more complex and therefore more challenging to characterize.

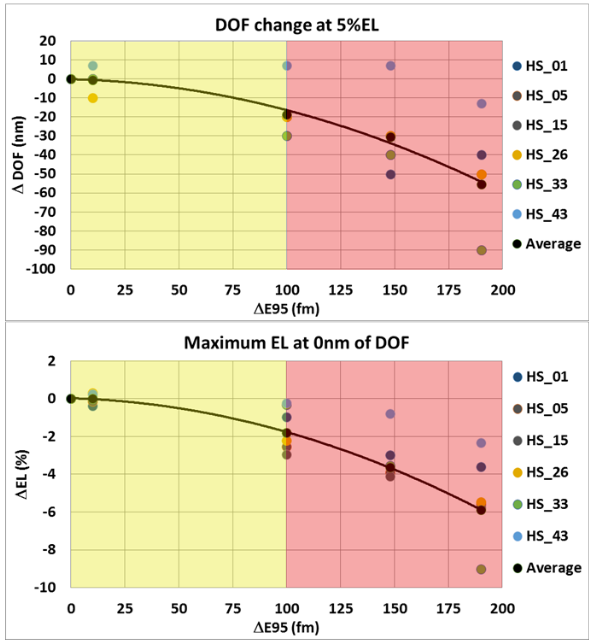

Figure 8. Hot spots Depth Of Focus (DOF) and Exposure Latitude (EL) change

In addition, for each hot spot, the maximum Depth Of Focus (DOF) at 5% Exposure Latitude (EL) and the maximum EL were investigated as functions of E95 bandwidth. A consistent response is observed: both DOF and EL tend to reduce as the E95 bandwidth increases. As shown in Figure 8, a 100fm of E95 changes from nominal condition represents a threshold point which separates two different regimes of sensitivity. . For ΔE95 < +100fm, the CD response is in the range of -1.0 nm/50fm whereas for ΔE95 > 100fm, a CD change of -2.0 nm/50fm is observed.

The sensitivity of CD Uniformity (CDU) to E95 bandwidth was also studied. For each E95 set point condition, a wafer was exposed at best dose and focus. CD-SEM measurements were made at 24 positions inside each exposure field of a central 5x5 exposure field matrix for a total of 600 measures per wafer. As noted in the PW analysis, changes in CDU were observed to be structure specific on top of a general degradation with increasing E95 bandwidth (Figure 9.)

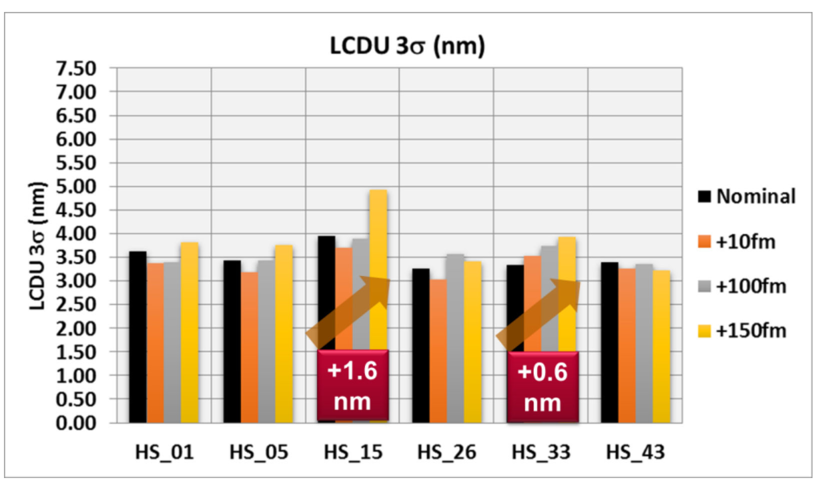

Figure 9. CD Uniformity per hot spot

2.5 Tip-to-Tip

As good overlap of Metal 1 extension over Via0 is required to minimize power distribution loss, characterization of "line end shortening" in printed features was performed. To measure the changes in Tip-to-Tip distance as a function of E95 bandwidth [12], a target of fixed gap of 80 nm was chosen. For each E95 set point condition, a wafer was exposed at best dose and focus. Per exposure field, 252 measurements were made for a total of 6,300 points for each wafer. A CD sensitivity of 2.5nm / 50fm E95 bandwidth was quantified, measuring at the same time a meaningful degradation of CD uniformity.

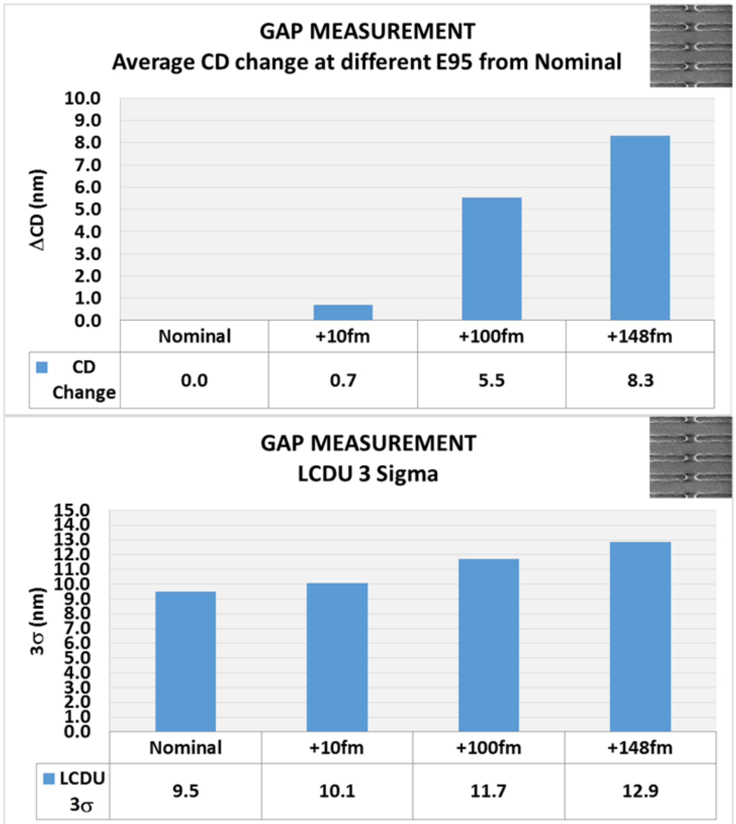

Figure 10. Tip-to-Tip gap measurement

2.6 CD Contour Analysis

In multiple patterning lithographic flows, the difference between the position of the center of a resist pattern from the nominal (designed) center position, also defined as Pattern Placement Error (PPE) is considered a critical area[13-14] for process monitoring and control. As measurement of single patterning quality at the edge of features is complex, the contours were extracted using Hitachi's Design Gauge Analyzer software. These contours were used to estimate the interaction between the printability responses of each individual feature edge as a function of changes in E95 bandwidth. The contour analysis was performed using the OPC design and not the effective lithography design target.

The analysis was performed using an averaging of 25 measurements per each wafer sample exposed (at fixed dose and focus) for two of the hot spot structures: HS#1, HS#5and HS#15. The nominal contour of each feature was compared to the contour from the exposure at +100fm E95 bandwidth. Changes in contour were detected with a sensitivity of 0.1nm and were classified according three different groups (or BINs).

BIN_0 : Measurement changes between 0 nm and |1| nm;
BIN_1 : Measurement changes between |1| nm and |2| nm;
BIN_2 : Measurement changes larger than |2| nm.

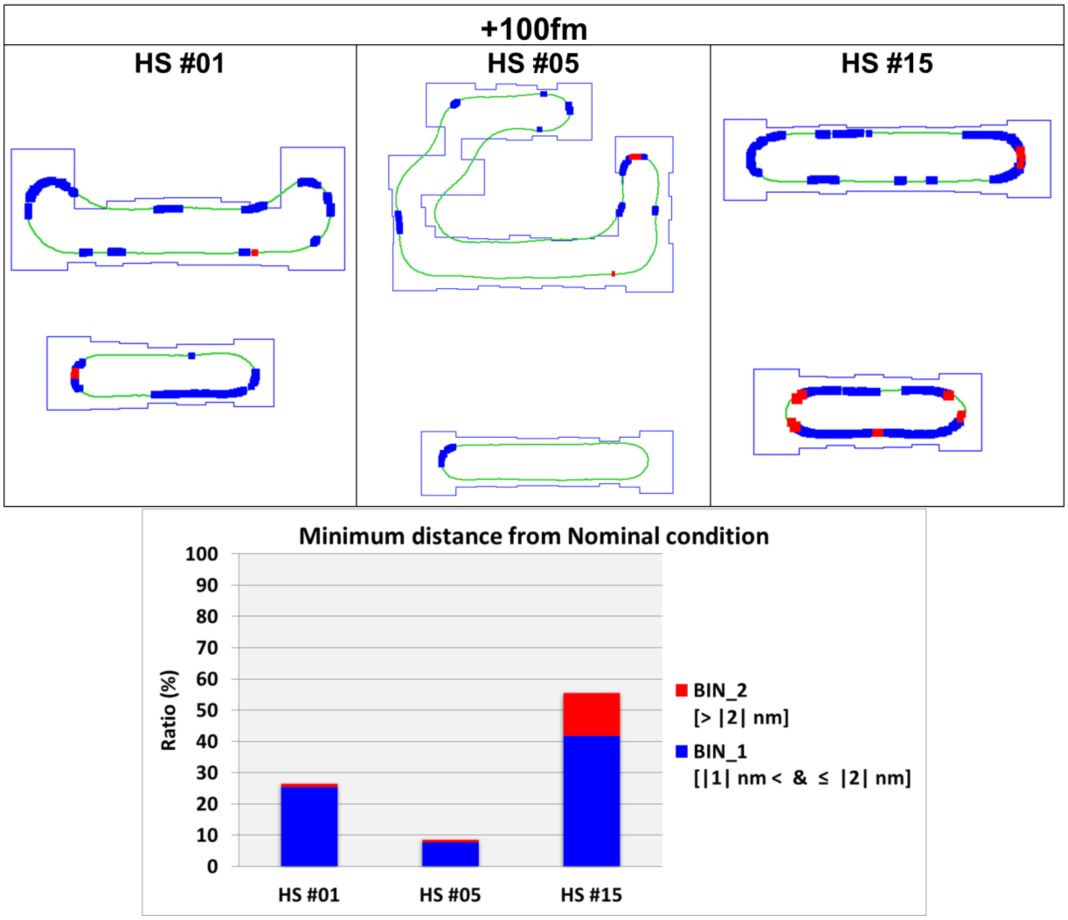

Figure 11. Contour analysis: Nominal vs +100fm

Figure 11 shows different responses between the selected hot spots, with some similarities in the trends observed. BIN_0 [>0 nm & < |1| nm] has not been reported since this bin can be considered a measurement noise. Hot spot HS#15 has twice the percentage of measurement points between |1| nm and |2| nm compared to HS#01, suggesting a much higher E95 sensitivity.

2.7 Line Width Roughness (LWR)

Line width roughness is of significant concern in device manufacturing as demonstrated by the ITRS defined roughness specification for low-frequency (LF) edge variation along lines.
The LWR measurements were carried out on the anchor feature: a Line-Space structure with a CD of 45nm and Pitch of 96nm, and an ADI target for 39nm trenches. Best dose and focus were determined to be at 39.5 mJ/cm^2 and -0.01µm. Per experimental E95 bandwidth condition, 9 measurements were made for each exposure field for a total of 567 samples for each wafer. Trench roughness was measured on a Hitachi CG5000 CD-SEM, applying the following settings:

- Magnification: 200k x 49k;
- TV mode 32 frames, 512 x 512 pixels;
- 400 measurement points along the line;
- Box length: 400 pixels;
- 5 lines measured per picture, 3 positions/pictures per grating, sum lines 4, smoothing 7, threshold 70%.

The measurements are made over a 2.15 micron trench length even though the FOV is 2.76 micron as the measurement box cannot go to the edge of the image.

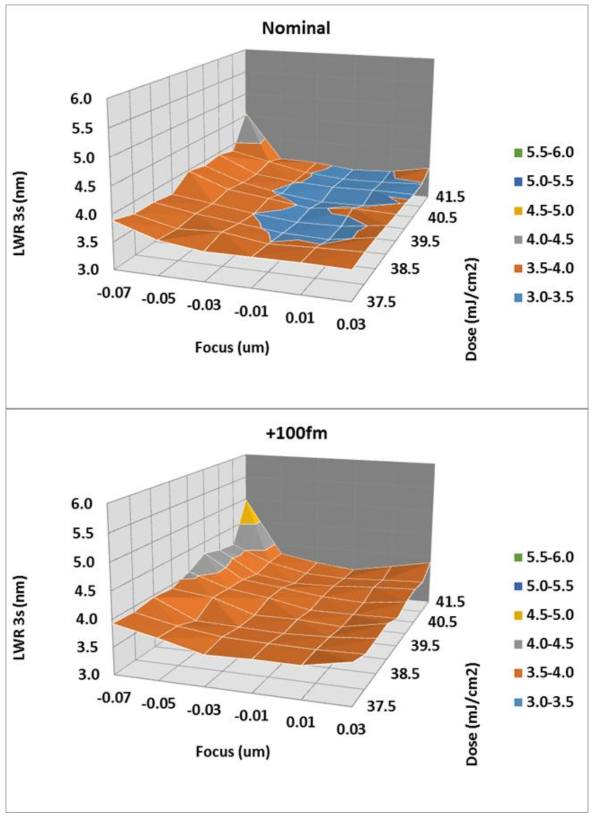

Figure 12. LWR: measure in spatial domain across FEM

To detect a change in the spatial domain of LWR (from 0.5nm to 1nm), a significant change in E95 bandwidth from nominal is required (ΔE95 $\geq$ 100 fm).

2.8 Assessment of E95 Bandwidth < 300 fm

Using Cymer's modulation capabilities, E95 bandwidth can be decreased compared to nominal 300fm performance. In this study, a minimum E95 bandwidth value of 200fm was obtained. As noted previously, this study reports the first experimental work on the effect of lower bandwidths (E95 < 300fm) on advanced node patterning performance.

In theory, a reduction in E95 bandwidth should increase the contrast and therefore improve the imaging process. Figure 14 is showing changes in shape of the process window exposed at 200fm; a modest increment of the exposure latitude and a minimal decrement in depth of focus are noted

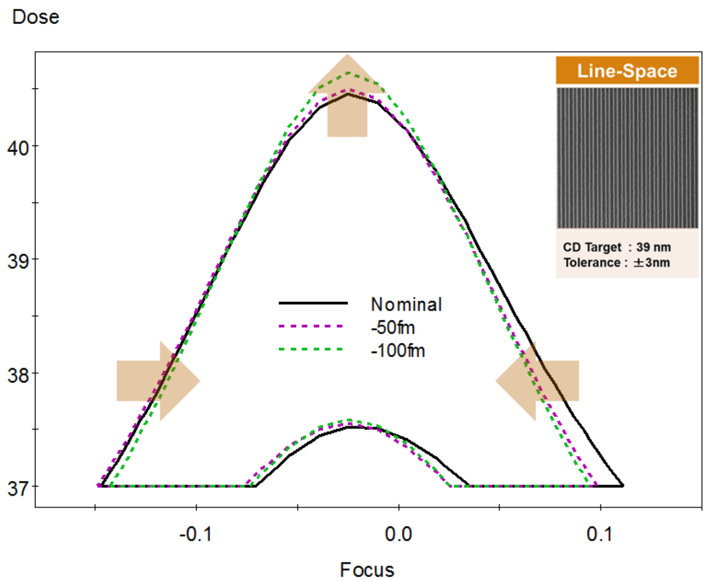

Figure 14. Anchor feature process window change at 250fm and 200fm

Similar to the results from the increased E95 bandwidth experiments, the hot spots have different responses and sensitivities to lower E95 bandwidth levels. Specifically, for large negative changes from nominal conditions (-100fm $\geq \Delta$E95 $\geq$ -50fm), each hot spot has a different rate of change per E95 bandwidth in terms of DOF and EL.

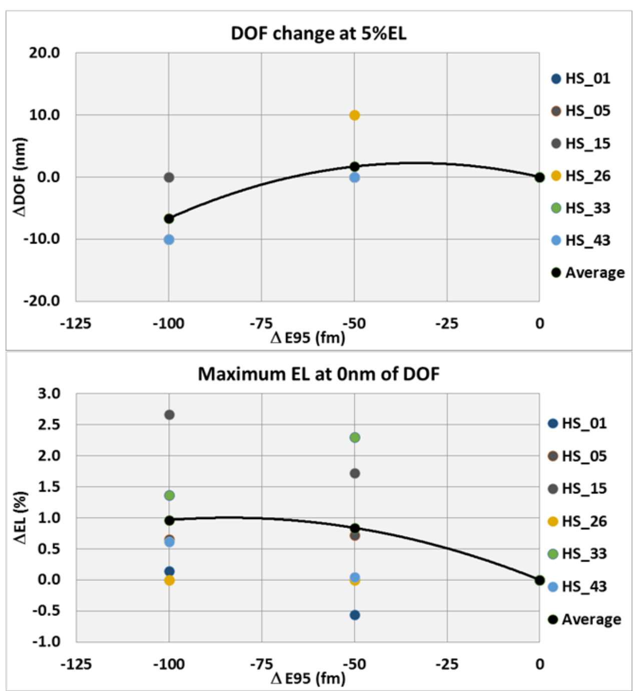

Figure 15. Hot spot Depth Of Focus (DOF) and Exposure Latitude (EL) changes (E95 < 300fm)

Initial analysis of the reduced E95 bandwidth setting results does not show a consistent process performance response; for example, features like HS15 show an improvement in contrast. Similar to the contour analysis at Nominal +100fm, the Nominal -100fm contour analysis shows responses in similar areas of the features: a reduction in E95 generating a CD change due to line ends shortening.

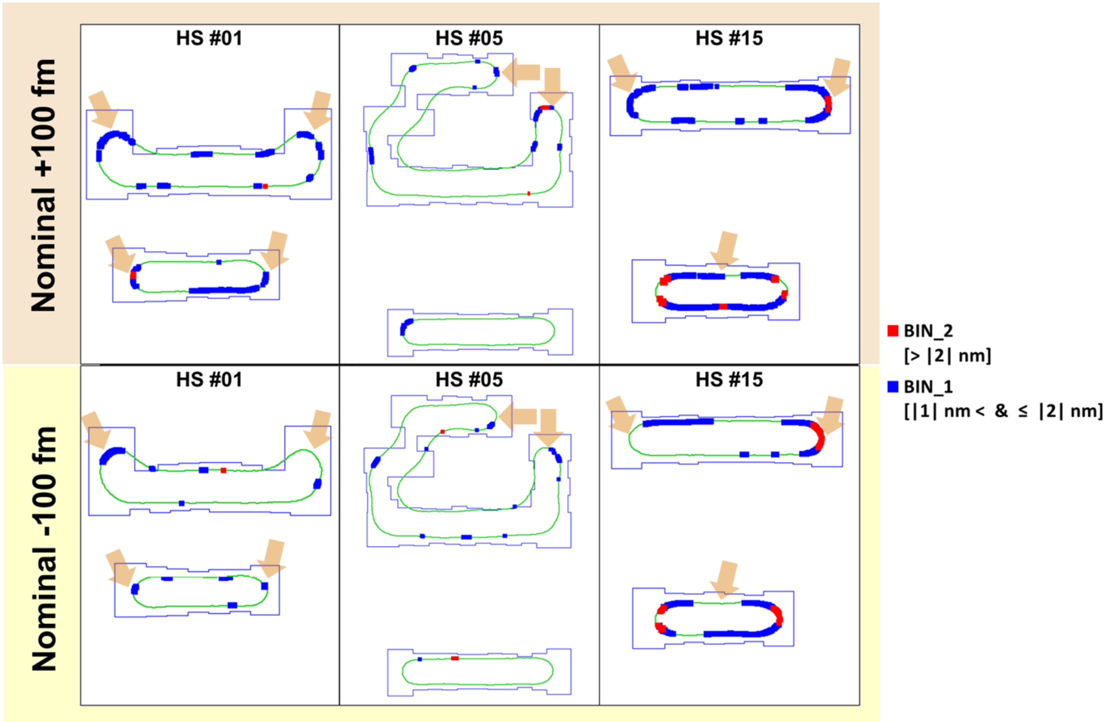

Figure 16. Contour analysis: Nominal vs -100fm and +100fm

While the responses to the E95 bandwidth changes occur at the same, specific areas, it is important to note that the magnitudes of the changes are different. This would suggest that the complexity of the 2D features analyzed and the fact that the OPC model for the imec N10 Metal 1 process was created at a nominal bandwidth of 300fm suggest that further studies are required to fully comprehend the pros and cons of E95 bandwidth changes on process window and other imaging metrics

3 SUMMARY AND CONCLUSIONS

In this work the impact of E95 bandwidth on N10 Metal 1 Logic features was studied. An investigation of six representative hot spot revealed complex, structure specific responses. E95 bandwidth induced CD changes can vary between –1.0nm CD / 50fm E95 to -2.0nm / 50fm depending on the hot spot structure. CDU responses were also determined to be structure specific, with some hot spots showing limited, if any, response to E95 bandwidth modulation. From roughness measurements in the spatial domain, a transition point at +100fm of E95 deviation from nominal conditions was identified; at this level the LWR change was estimated in the range of 0.5nm to 1nm.

Furthermore, line-end shortening in a line-space matrix and differences in pattern placement errors were studied. The distance between two line-ends showed a sensitivity of 2.5 nm CD /10 fm E95. Using contour analysis it was possible to study the response of pattern placement error (PPE), which is dependent on the feature complexity and OPC correction applied. Through the contour analysis, it can be estimated that some areas of the features have a sensitivity of -0.3 nm/10fm.

Based on the results of this investigation, a patterning response to lower E95 Bandwidth settings (200fm and 250fm) can be observed in terms of process window impacts: an increase in the exposure latitude and a reduction in the DOF are noted.

The significant hot spot dependent responses observed demonstrate the complexities that must be considered when changing imaging conditions and certainly requiring further study to identify the pros and cons of operating at lower E95 bandwidth values.

ACKNOWLEDGMENTS

The authors would like to thank Nadia Vandenbroeck, Christina Baerts, Sandip Halder for the assistance in several measurements performed in imec. Aleks Simic, Remo Petrella (Cymer), Osamo Inoue and Takashi Ishizawa (Hitachi) are thanked for providing technical support. Herman Godfried (ASML Veldhoven), and Jason Lee and James Bonafede (Cymer) are thanked for fruitful technical discussions. Ivan Lalovic is thanked for support in the initial project definition.

REFERENCES

[1] ITRS, International Technology Roadmap for Semiconductors, http://www.itrs.net.
[2] J.Choi et al., "Enhancing lithography process control through advanced, on-board beam parameter metrology for wafer level monitoring of light source parameters,", Proc. SPIE Optical Microlithography XXV 8236,99 (2012).
[3] P.Alagna et al., "Lithography imaging control by enhanced monitoring of light source performance", Proc. SPIE 8683, Optical Microlithography XXVI, 86830S (2013).
[4] P.Alagna et al., "Improving On-Wafer CD Correlation Analysis Using Advanced Diagnostics and Across-Wafer Light-Source Monitoring", Proc. SPIE 9052, Optical Microlithography XXVII, 905228 (2014).
[5] J.Choi et al., "Enhancing lithography process control through advanced, on-board beam parameter metrology for wafer level monitoring of light source parameters,", Proc. SPIE Optical Microlithography XXV 8236,99 (2012).
[6] M. van den Brink, "Many ways to shrink: The right moves to 10 nanometer and beyond", SPIE Photomask Technology (2014).
[7] U. Iessi ed al. "Laser bandwidth effect on overlay budget and imaging for the 45 nm and 32nm technology nodes with immersion lithography", Proc. SPIE 7973, Optical Microlithography XXIV, 797328.
[8] N. Seong, et al. "Analysis of the effect of laser bandwidth on imaging of memory patterns", Proc. SPIE 7140, Lithography Asia 2008, 714042.
[9] P. De Bisschop et al. "Impact of finite laser bandwidth on the CD of L/S structures", Journal of Micro / Nanolithography, MEMS and MOEMS (JM3), Vol. 7, No. 3 (2008).
[10] N. Seong, et al. "Analysis of the effect of laser bandwidth on imaging of memory patterns", Proc. SPIE 7140, Lithography Asia, 714042 (2008).
[11] W. Conley et al. "Impact of bandwidth on contrast sensitive structures for low k1 lithography", Proc. SPIE 9426-6, Optical Microlithography XXVIII, (2015).
[12] R.C. Peng et al. "Effects of laser bandwidth on Iso-Dense Bias and Line End Shortening at sub-micron process nodes", Proc. of SPIE Vol. 6520, Optical Microlithography XX, 65203S, (2007).
[13] D. Fuchimoto et al, "Measurement Technology to Quantify 2D Pattern Shape in sub-2x nm Advanced Lithography", Proceeding of SPIE 86810A,2014
[14] D. Fuchimoto et al, "Contour-based metrology for complex 2D shaped patterns printed by multiple-patterning process", Proceeding of SPIE 9050-30,2013

http://dx.doi.org/10.1117/12.2085823